LISTING OF CLAIMS

Claims 1-17 (canceled)

18. (Currently amended) A semiconductor substrate having an array of die areas with integrated circuits and kerf areas with fill patterns comprised of:

(a) a patterned conducting layer forming portions of semiconductor devices and a patterned fill layer in said kerf areas, wherein spacing between said patterned fill layers and said die areas is not greater than about 2 micrometers;

(b) a spin-on-glass layer over said patterned conducting layer, wherein said patterned fill layer in said kerf areas results in a uniform coating of said spin-on-glass layer over corners of said array of die areas, and said spin-on-glass layer converted to a silicon oxide by curing, and chemically-mechanically polished back to form a planar silicon oxide layer;

(c) an insulating layer on said silicon oxide layer;

the structure described in elements (a) through (c) formed for each additional patterned conducting layer, one upon the other, required for said integrated circuit.

19. (Original) The structure of claim 18, wherein said conducting layer is a metal.

20. (Original) The structure of claim 19, wherein said metal is aluminum deposited to a thickness of between about 6000 and 10000 Angstroms.

21. (Withdrawn) The structure of claim 18, wherein spacing between said patterned fill layers and said die areas is not greater than about 2 micrometers.

22. (Original) The structure of claim 18, wherein said kerf areas have a width of between about 120 and 600 micrometers between said die areas.